

# C.U.SHAH UNIVERSITY

## Summer Examination-2017

Subject Name: Digital VLSI Design

Subject Code: 5TE01DVD1

Branch: M.Tech (VESD)

Semester: 1

Date: 30/03/2017

Time: 10:30 To 01:30

Marks: 70

### Instructions:

- (1) Use of Programmable calculator and any other electronic instrument is prohibited.
  - (2) Instructions written on main answer book are strictly to be obeyed.
  - (3) Draw neat diagrams and figures (if necessary) at right places.
  - (4) Assume suitable data if needed.
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### SECTION – I

- Q-1** Define the following terms. (07)
- a. Accumulation in MOS transistor
  - b. Depletion in MOS transistor
  - c.  $V_{OH}$
  - d. Propagation delay
  - e. Switching characteristics
  - f.  $V_{IL}$
  - g.  $V_{OL}$

- Q-2** Attempt all questions (14)
- (a) Explain Transmission Gate Characteristics TG-based Switch Logic.
  - (b) Derive Equation of  $V_{IH}$  for CMOS inverter.

OR

- Q-2** Attempt all questions (14)
- (a) Explain D type Flip Flop using Transmission Gate.
  - (b) Derive Equation of  $V_{TH}$  for CMOS inverter.

- Q-3** Attempt all questions (14)
- (a) Explain RC Delay for CMOS and Elmore Delay.
  - (b) Explain constant field scaling device reduction strategy and show that the power density does not change in a device scaled using this technique.

OR

- Q-3** Attempt all questions (14)
- (a) Draw input and output waveforms during high to low transition of output for a CMOS inverter. Derive expression for  $T_{PHL}$ .
  - (b) Explain MOSFET Switch Logic in detail.



## SECTION – II

- Q-4**      **Define the following terms.**      **(07)**
- a. Bi-CMOS
  - b. Pull-up Device.
  - c. Pass Transistor
  - d. Pull-down device.
  - e. TSPC.
  - f. Pseudo Gate.
  - g. Define Bi-CMOS.

- Q-5**      **Attempt all questions**      **(14)**
- (a) Draw and explain Multiple-Output Domino Logic.
  - (b) Explain CMOS SR Flipflop using NAND implementation.

**OR**

- Q-5**      **Attempt all questions**      **(14)**
- (a) Explain in detail Single-Phase Logic using MOS.
  - (b) Write a note on Pre-charge and Evaluate logic for dynamic logic circuits.

- Q-6**      **Attempt all questions**      **(14)**
- (a) Write a note on NORA Logic.
  - (b) Explain Logic '0' Transfer for pass transistor.

**OR**

- Q-6**      **Attempt all Questions**      **(14)**
- (a) What is the need of voltage bootstrapping? Discuss Voltage bootstrapping in detail.
  - (b) Draw and explain Schmitt Trigger Circuits using MOS.

